## REMARKS

By this Amendment, Applicants amend claims 1 and 17.

Accordingly, claims 1-21 remain pending in the application.

Applicants respectfully request that the Examiner provide a new, non-final Office Action that clearly identifies where in the prior art each of the features of claims 1-21 are supposedly disclosed. Reexamination and reconsideration are also respectfully requested in view of the following Remarks.

## REQUEST FOR NEW NON-FINAL OFFICE ACTION

M.P.E.P. § 706.02(j) provides that:

> "35 U.S.C. 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references. After indicating that the rejection is under 35 U.S.C. 103, the examiner should set forth in the Office action: (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) the difference or differences in the claim over the applied reference(s), (C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification."

Here, the Office Action fails to meet these requirements. In particular, the Office Action fails to specifically identify with respect to each claim: (1) the difference or differences in the claim over Williams or Contiero, (2) the proposed modification of Williams or Contiero necessary to arrive at the claimed subject matter, and (3) an explanation why one of ordinary skill in the art at the time the invention was made

would have been motivated to make the proposed modifications. Instead, the Office Action just generally averts that "one skilled in the art would be motivated to combine these references." However, this wholly fails to explain exactly **how** the Examiner is proposing to combine the references, i.e., what parts of Williams are supposed to be combined with what parts of Contiero to supposedly produce each of the various claims.

Additionally, the Office Action fails to even mention numerous features of Applicants' claims (e.g., "a drain region aligned to outer walls of the looped insulating patterns," "a pickup region of the first conductivity type disposed adjacent to the heavily doped source layer disposed in an upper portion of the epitaxial layer of the body region," "a plurality of drain electrodes connected to the drain region, wherein the high voltage is supplied to the drain electrodes," etc.). In other cases, the Office Action states without any support or citation whatsoever that the references disclose certain claimed features (e.g., "where the gate array is essentially mesh-shaped structure").

In summary, the Office Action fails to fairly advise and put Applicants on notice of the basis of the rejections of claims 1-21. Applicants are left in a position of trying to guess where the Examiner may be finding various features of Applicants' claims in the cited references, and why he believes there would have been a suggestion for the proposed modifications and combinations in the prior art or knowledge generally available to one of ordinary skill in the art at the time the invention was made. Applicants should not be forced to guess as to the basis of claim rejections. Nor should Applicants be forced to resort to filing a Notice of Appeal to the Board of Patent Appeals in order to receive a clear and concise explanation of the rejections of Applicants claims, as provided for by M.P.E.P. §§ 706.02(j) and 707.07.

Accordingly, Applicants respectfully request a new, non-Final Office Action that fulfils the requirements of M.P.E.P. §§ 706.02(j) and 707.07 for each and every one of Applicants' claims.

## 35 U.S.C. § 103

The Office Action rejects claims 1-21 under 35 U.S.C. § 103 over Williams et al. U.S. Patent 5,485,027 ("Williams") in view of Contiero et al. U.S. Patent 5,126,911 ("Contiero"). Applicants respectfully traverse those rejections for at least the following reasons.

## The Proposed Combination of Williams and Contiero

Applicants respectfully traverse the proposed combination of Williams and Contiero with respect to each and every one of the claims 1-21 for at least the following reasons.

At the outset, as explained above, the Office Action wholly fails to explain exactly **how** the Examiner is proposing to combine the references, i.e., what parts of Williams are supposed to be combined with what parts of Contiero to supposedly produce each of the various claims.

Furthermore, Applicants respectfully submit that the Office Action has failed to provide any suggestion or motivation in the prior art for the proposed combination. Applicants also respectfully note that such a suggestion or motivation must be supplied for each and every element to be imported from one reference and combined into another reference for each one of the claims 1-21.

Specifically, M.P.E.P. § 2142 states that "there must be some suggestion or motivation, **either in the references themselves or in the knowledge generally available to one of ordinary skill in the art**, to modify the reference or to combine reference teachings" (emphasis added). Similarly, M.P.E.P. § 2143.01 provides that:

> "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so **found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art**."

(emphasis added).

A simple inspection of the Office Action clearly reveals that there is absolutely no citation to anything in the references themselves or anywhere else in the prior art supporting the proposed motivation. Meanwhile, a rejection under 35 U.S.C. § 103 must be based on objective evidence of record, and cannot be supported merely on subjective belief and unknown authority. M.P.E.P. § 2144.03 provides that:

> "there must be some form of evidence in the record to support an assertion of common knowledge. See In re Lee, 277 F.3d at 1344-45, 61 USPQ2d at 1434-35 (Fed. Cir. 2002); Zero, 258 F.3d at 1386, 59 USPQ2d at 1697 (holding that general conclusions concerning what is "basic knowledge" or "common sense" to one of ordinary skill in the art without specific factual findings and some ***concrete evidence in the record to support these findings*** will not support an obviousness rejection)."

(Emphasis added). See also In re Lee, 277 F.3d at 1343-44, 61 USPQ2d at 1433-34 (Fed. Cir. 2002) (the examiner's finding of whether there is a teaching, motivation or suggestion to combine the teachings of the applied references must not be resolved based on "subjective belief and unknown authority," but must be "based on objective evidence of record.").

No such concrete evidence has been provided by the Examiner here. Nor did the Examiner submit an affidavit as required by 37 CFR 1.104(d)(2) if this proposed motivation were based on facts within his personal knowledge (see MPEP § 2144.03). Applicants request such an affidavit if this rejection continues to be maintained based a motivation for combination not explicitly suggested in the prior art.

Therefore, for these reasons, Applicants respectfully submit that the supposed motivation for combining the references fails to meet the requirements of M.P.E.P. §§

2142, 2143.01 and 2144.03.

Accordingly, for at least these reasons, Applicants respectfully traverses the proposed combination of references with respect to each of the claims 1-21, and respectfully request that it be withdrawn.

Claim 1

Among other things, the array of claim 1 at least one common electrode for the one of the source or drain commonly shared among the N DMOS transistors, and at least one unique electrode for the one of the source or drain of each of the double diffused MOS transistors that is formed unique to each of the DMOS transistors.

The Office Action makes no mention of these features, which were previously recited in claim 17.

Applicants respectfully submit that the cited prior art does not disclose or suggest an array including these features in combination with the other features of claim 1.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over the prior art.

Claims 2-3 and 16-21

Claims 2-3 and 16-21 depend from claim 1 and are therefore deemed patentable for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claims 2 & 3

Claims 2 and 3 are drawn to pull-up transistor arrays that include, respectively, an nVDMOS transistor and a pLDMOS transistor, arranged in the epitaxial layer, wherein one of a source or drain of each double diffused MOS transistor is formed unique to each transistor, and wherein the N DMOS transistors share in common the other of the source or drain.

The Office Action fails to cite anything in either Williams or Contiero that discloses the recited nVDMOS transistor or pLDMOS transistor, including all of the recited features. Nor has the Office Action explained how one of ordinary skill in the

art at the time the invention was made could have combined the references to produce the claimed device including, respectively, these transistors, and what teaching or suggestion in the prior art would have suggested that they do so.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claims 2 and 3 are patentable over the prior art.

Claim 18

Among other things, in the array of claim 18, the epitaxial layer is of a first conductivity type and the source and drain are of a second conductivity type different from the first conductivity type.

The Office Action fails to cite anything in either Williams or Contiero that discloses such features, in combination with all of the other features of claim 1. Nor has the Office Action explained how one of ordinary skill in the art at the time the invention was made could have combined the references to produce the claimed device, and what teaching or suggestion in the prior art would have suggested that they do so.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 18 is patentable over the prior art.

Claim 21

Among other things, the array of claim 21 includes at least 3 DMOS transistors laterally arranged in an epitaxial layer, wherein the at least 3 DMOS transistors share in common either a source or a drain.

The Office Action fails to cite anything in either Williams or Contiero that discloses such features, in combination with all of the other features of claim 1. Nor has the Office Action explained how one of ordinary skill in the art at the time the invention was made could have combined the references to produce the claimed device, and what teaching or suggestion in the prior art would have suggested that they do so.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 21 is patentable over the prior art.

Claim 4

Among other things, the pull-up transistor array of claim 4 includes: (1) a plurality of looped insulating patterns regularly spaced and disposed on the epitaxial layer along one direction; (2) a gate pattern disposed on an upper part of a region surrounded by the looped insulating pattern such that the gate pattern partially overlaps an upper portion of the looped insulating layer, and having a mesh-shaped structure in which with a plurality of openings are arranged two-dimensionally exposing the epitaxial layer; and (3) a drain region aligned to outer walls of the looped insulating patterns to be disposed vertically in the epitaxial layer between the looped insulating patterns.

Applicants respectfully submit that the cited references do not disclose or suggest any pull-up transistor array including such a combination of features.

At the outset, the Office Action completely fails to mention the feature wherein a drain region is aligned to outer walls of the looped insulating patterns to be disposed vertically in the epitaxial layer between the looped insulating patterns. Applicants respectfully submit that the cited references, taken alone or collectively, do not include such a feature. And specifically, if the field isolation regions are supposed to correspond to such looped insulating patterns, clearly FIG. 4 of Contiero does not show a drain region aligned to outer walls of the looped insulating patterns.

Therefore, it is not possible for any combination of the cited references to produce the device of claim 4.

Furthermore, Applicants respectfully traverse the statement in the Office Action that the field oxide layers of Contiero "can be considered" a plurality of looped insulating patterns regularly spaced and disposed on the epitaxial layer along one direction. Applicants see nothing in Contiero that makes such a disclosure or suggestion.

Finally, the Office Action states without any citation or support that the "gate array" of Contiero has a "mesh-shaped structure." First off, claim 4 recites a "gate pattern" not a "gate array." Second, there is nothing in Contiero that discloses or

suggests that any gate pattern has any mesh-shaped structure. Indeed, to the contrary, FIG. 4 of Contiero clearly shows that there are two independent gate structures (G1 and G2) interleaved on a same layer, and driven with different gate voltages (see FIG. 1) such that no mesh-shaped structure would even seem possible!

Accordingly, for at least these reasons, Applicants respectfully submit that claim 4 is patentable over the prior art.

Claims 5-9

Claims 5-9 depend from claim 4 and are deemed patentable for at least the reasons set forth above with respect to claim 4, and for the following additional reasons.

Claim 6

Among other things, in the pull-up transistor array of claim 6, each source region comprises: (1) a body region of the first conductivity type disposed in the epitaxial layer of each opening; (2) a heavily doped source layer of the second conductivity type disposed in an upper portion of the epitaxial layer in the body region of the first conductivity type; and (3) a pickup region of the first conductivity type disposed adjacent to the heavily doped source layer disposed in an upper portion of the epitaxial layer of the body region.

The Office Action fails to cite anything in either Williams or Contiero that discloses such features, in combination with all of the other features of claim 4, particularly the pickup region of the first conductivity type disposed adjacent to the heavily doped source layer disposed in an upper portion of the epitaxial layer of the body region of the first conductivity type. Nor has the Office Action explained how one of ordinary skill in the art at the time the invention was made could have combined the references to produce the claimed device, and what teaching or suggestion in the prior art would have suggested that they do so.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 6 is patentable over the prior art.

Claim 10

Among other things, the pull-up transistor array of claim 10 includes: (1) looped gate patterns respectively disposed on the epitaxial layer, wherein the looped gate patterns overlap an upper portion of sidewalls of the first conductivity type well; (2) a looped insulating pattern interposed between the epitaxial layer and the looped gate patterns; (3) a source region aligned to outer walls of the looped insulating patterns, disposed in the second conductivity type well; and (4) a plurality of drain regions aligned to inner walls of the looped insulating patterns, respectively disposed in the first conductivity type well

Applicants respectfully submit that the cited references do not disclose or suggest any pull-up transistor array including such a combination of features.

At the outset, the Office Action completely fails to mention the features wherein a source region is aligned to outer walls of the looped insulating patterns, and a plurality of drain regions are aligned to inner walls of the looped insulating patterns. Applicants respectfully submit that the cited references, taken alone or collectively, include such a feature. And specifically, if the field isolation regions are supposed to correspond to the looped insulating patterns, clearly FIG. 4 of Contiero does not show a source region aligned to outer walls of the looped insulating patterns and a plurality of drain regions aligned to inner walls of the looped insulating patterns.

Therefore, it is not possible for any combination of the cited references to produce the device of claim 10.

Furthermore, Applicants respectfully traverse the statement in the Office Action that the field oxide layers of Contiero "can be considered" a plurality of looped insulating patterns regularly spaced and disposed on the epitaxial layer along one direction. Applicants see nothing in Contiero that makes such a disclosure or suggestion.

Finally, the Office Action fails to even mention the looped gate patterns of claim 10. Therefore, it is not possible for any combination of the cited references to produce the device of claim 10.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 10 is patentable over the prior art.

Claims 11-15

Claims 11-15 depend from claim 10 and are deemed patentable for at least the reasons set forth above with respect to claim 10, and for the following additional reasons.

Claim 11

Among other things, in the pull-up transistor array of claim 11, the source region includes: (1) a heavily doped diffusion layer of the first conductivity type formed in an upper portion of the epitaxial layer in the second conductivity type well; and (2) a pickup region of the second conductivity type, wherein the source layer of the first conductivity type surrounds the pickup region of the second conductivity type.

The Office Action fails to cite anything in either Williams or Contiero that discloses such features, in combination with all of the other features of claim 10, particularly the pickup region of the second conductivity type surrounded by the source layer of the first conductivity type. Nor has the Office Action explained how one of ordinary skill in the art at the time the invention was made could have combined the references to produce the claimed device, and what teaching or suggestion in the prior art would have suggested that they do so.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 11 is patentable over the prior art.

Claim 13

Among other things, the pull-up transistor array of claim 13 includes drain electrodes connected to the drain regions to output a high voltage.

The Office Action fails to cite anything in either Williams or Contiero that discloses such features, in combination with all of the other features of claim 10. Nor has the Office Action explained how one of ordinary skill in the art at the time the

invention was made could have combined the references to produce the claimed device, and what teaching or suggestion in the prior art would have suggested that they do so.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 13 is patentable over the prior art.

## CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-21, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

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By: _____

Kenneth D. Springer
Registration No. 39,843

VOLENTINE FRANCOS & WHITT, P.L.L.C.
One Freedom Square
Suite 1260
11951 Freedom Drive
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740